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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/419,523	10/18/1999	PAUL PETERSEN	MICE-0051-US	1377

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EXAMINER	
CHACE, CHRISTIAN	
ART UNIT	**PAPER NUMBER**
2189	

DATE MAILED: 05/30/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/419,523	PETERSEN, PAUL	
	Examiner	Art Unit	
	Christian P. Chace	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 April 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *41-51,53-60,62-65 and 67* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *41-51,53-60,62-65 and 67* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

This Office action has been issued in response to amendment filed 27 April 2006. Claims 41-51, 53-60, 62-65, and 67 are pending. Applicant's arguments have been carefully and respectfully considered, but they are not persuasive. Accordingly, this action has been made FINAL.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 41-51, 53-60, 62-65 and 67 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. With respect to independent claims 41, 54, and 62, the newly added limitations do not appear to be enabled by the instant specification. For example, while the instant specification literally recites the determining a maximum number of memory devices that can be supported per memory bus channel (independent claim 41), the instant specification does not appear to discuss how to do so, and it does not appear that one of ordinary skill in the art would know how to make and/or use it; as applicant is claiming this limitation (it is part of the invention). Independent claim 54 has a similar limitation added, as does independent claim 62.

The remaining claims depend upon the instant claims, and are rejected for at least the reasons discussed supra with respect to the claims upon which they depend.

Claims 41-51, 53-60, 62-65 and 67 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The determining steps added to the instant independent claims as discussed supra do not appear to be described in sufficient detail to clearly allow persons of ordinary skill in the art to recognize what he or she has claimed. Accordingly, this brings into question whether applicant had possession of the claimed invention at the time the instant application was filed.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 41-42, 45, 48-49, 51, 53-55, 58-60, 62-65, and 67 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arai (US Patent # 5,280,599), with RAMBUS Direct RMC.d1 Data Sheet (8/7/98) offered as extrinsic evidence of inherency, and Yoshizawa et al (US Patent # 5,787,464).

With respect to claims 41, 54, and 62, examiner notes that the definition of "memory configuration information," in page 5 of the instant specification and shown in figure 3, is defined as, "type, amount, and operating characteristics of memory." "Residual memory capacity" is defined as the difference between existing memory and maximum possible memory expansion.

Obtaining memory configuration information of a computer system, or, the actual memory of the system, determining a memory capacity of the system, or, the possible memory allowed in the system, and determining memory upgrade options based on a residual memory capacity of the computer system is disclosed in column 2, lines 46-60. Examiner notes that "upgrade options" and "memory characteristics" are very broad in scope, and have been interpreted as such by examiner.

"Executing a software routine to determine a maximum number of memory devices that can be supported per memory bus channel of the computer system," is disclosed on the top of page 40 of RAMBUS, as address values are programmed into configuration fields to determine total device size. Page 41 discusses configuration. Page 42 discusses initialization (software routine) that determines present devices. Page 40 discusses that a device field has been programmed at 5-bits, therefore allowing a maximum of 32 devices per stick. Pages 56-58 further discuss configuration and RDRAM initialization. Also, see page 73, which discusses the algorithm InitDev. The system must determine whether it is actually there or not (characteristic other than size). It being present or not will inherently affect the capacity. This is discussed in RAMBUS on page 1, which discloses the optional 1 to 32 RDRAMS that may be

connected to the controller, page 40, which discusses the configuration options (number of regions, e.g.), page 41, which discusses the addressing options based on the configuration, page 42, which discloses that initialization "automatically" manages the configuration, including whether a device is present or not, page 45, which elaborates on the mapping techniques, page 57, which shows the actual configuration commands for the number of devices present, and pages 72-75, which discuss initialization of the devices, including "serial presence detect," which applicants are also very strongly encouraged to review. In addition, examiner notes that the instant specification at the top of page 6 appears to admit the instant limitation as prior art.

The difference between the claims and Arai is the explicit recitation of expanding/replacing the number of memory devices.

Yoshizawa et al disclose expanding and replacing the number of memory devices in the abstract.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the invention, having the teachings of Arai and Yoshizawa et al before him/her, to utilize the expansion/replacement of Yoshizawa et al in the system of Arai as it allows for on-line expansion and replacement of memory modules, as disclosed by Yoshizawa et al in the abstract.

With respect to claims 42, 55, 63, and 65, the act of obtaining memory configuration information comprising obtaining an indication of an installed system memory amount is disclosed by Arai in column 2, lines 46-60.

With respect to claims 45 and 58, the act of obtaining memory configuration information comprising accessing a non-volatile storage device is disclosed by Arai in figure 3 as ROM/BIOS, and further discussed in column 3, lines 53-59.

With respect to claims 48-49, 59, and 64, obtaining the maximum number of memory devices and maximum amount of memory for the computer system are inherent, as the number of address bits, according to the binary number system upon which computers operate, indicate the "amount of memory" which includes the number of "devices." As evidence of inherency, examiner urges applicant to review Dresser et al (discussed below) in column 4, line 66 into column 5, line 1.

With respect to claim 51, providing memory upgrade options to a user is disclosed in column 6, line 45, which discusses a "window" for such information.

Examiner notes that the same obviousness statement and motivation is applicable to all claims noted supra as stated supra with respect to the claims upon which they depend.

With respect to claims 53, 60, and 67, the characteristic comprising a limit on the number of memory devices that can be installed on a memory channel regardless of the number of open slots is inherent, and, the RAMBUS reference discussed supra, particularly with respect to addressing, is evidence of such inherency – only so much space may be addressed by the number of address bits being used in the entire system – even if one memory slot has a 1 gigabit memory, but the other slots are all open, if that is the maximum memory addressable by the address bus, then that is the only memory that will work in the system.

Claims 43 and 56-57 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arai, Yoshizawa et al, and Helm et al (US Pat. # 5,129,069).

With respect to claims 43 and 56-57, Arai and Yoshizawa et al disclose the claimed invention upon which the instant claims depend.

The difference between the instant claim and Arai and Yoshizawa et al is that Arai and Yoshizawa et al, although disclosing a memory amount as shown supra, do not specifically disclose the configuration information comprising a number of memory module sockets.

Helm et al, however, disclose memory module "slots," which examiner interprets as "sockets," in figure 1.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention, having the teachings of Arai, Yoshizawa et al, and Helm et al before him/her, to obtain the "memory amount" disclosed by Arai and Yoshizawa, based on the number of "sockets" as disclosed in Helm et al, because, as discussed supra with respect to claims 8-9 , 17, and 20, the amount of memory in or available to the system is inherently dependent upon the number of address bits used in the system.

Claim 44 is rejected under 35 U.S.C. 103(a) as being unpatentable over Arai, Yoshizawa et al, and Cowell (US Pat. # 5,860,134).

Arai discloses the claimed invention upon which the instant claims depend.

The difference between the instant claim and Arai and Yoshizawa et al is that the memory configuration information comprises an operating speed of the installed system memory.

However, Cowell discloses a "type detection," which includes system bus speeds, in column 8, line 35 into column 9, line 35.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention, having the teachings of Arai, Yoshizawa et al, and Cowell before him/her, to utilize the type detection of Cowell in the system of Arai and Yoshizawa et al because the type detection signal allows the system to coordinate memory speeds according to the first and second type signals, as disclosed by Cowell, in column 9, lines 34-36, which increase the flexibility of the system, as made hackneyed in the state of the art.

Claims 46, 47, and 50 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arai, Yoshizawa et al, and Dresser et al (US Pat. # 5,446,860).

With respect to claims 46, 47, and 50, Arai and Yoshizawa et al disclose the claimed invention upon which the instant claims depend.

The difference between the instant claims and Arai and Yoshizawa et al is that the act of accessing a non-volatile storage device comprises accessing a serial presence detect device. The system of Arai and Yoshizawa et al operates serially. If a program to detect presence of a device is stored in ROM, as it is in BIOS, then it is, technically, a serial presence detect device.

However, assuming *arguendo,* that the above is not the case, Dresser et al disclose serial presence detect data in figure 4. Inherently, if there is serial presence detect data, there is a serial presence detect device to obtain said data, as computers need to be told what to do, so to speak.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention, having the teachings of Arai, Yoshizawa et al, and Dresser et al before him/her, to use the serial presence detect device to detect the serial presence of devices in the Arai and Yoshizawa et al system using the device of Dresser et al, because in search for the maximum amount of memory, the presence detect bits denote the maximum amount of memory, as disclosed by Dresser et al in column 4, lines 65-68. Examiner notes that SIMMs, as explicitly disclosed in Dresser et al, are dynamic random access memory devices and are inherently plugged into "slots," by definition. Applicant is invited to see figure 3 of Dresser et al and column 4, line 65 into column 6, line 65 for further discussion of same.

Response to Arguments

Any objections and/or rejections not repeated herein have been overcome by the instant amendment and withdrawn accordingly.

With respect to applicant's arguments regarding the 35 USC 112, 1st paragraph rejections, examiner is confused. The cited section of the specification still does not appear to discuss *how* the actual determination is made – loading information into a memory is extremely well-known to those of even rudimentary skill in the art. Applicant continues by discussing the RAMBUS ® controller information. This is what confuses

examiner – is that not admitted prior art? Applicant argues "prior knowledge" that there is a limit of 32 devices – what technique is applicant attempting to claim, that is not prior art, that determines this prior knowledge? There are only 32 slots in the physical channel for the noted controller does this constitute the "prior knowledge?" If so, is this not admitted prior art, then, as one of ordinary skill in the art can clearly count the slots in the applied data specification sheet reference? In other words, is the "determining" merely counting, then? Applicant does not discuss how the "determined" information is then put into a BIOS or other memory to be read out later – the process of how a BIOS routine would be "used" is also not discussed in the instant specification.

With respect to the arguments regarding the 35 USC 103 rejections, applicant appears to argue with respect to the 112 rejection that the instant specification enables the claim language because the RAMBUS system is disclosed. However, the RAMBUS system is prior art.

Arai uses a RAMBUS known system. The specification sheet discloses the particular claim limitations of that known system as discussed int eh body of the rejection. Applicant argues that "there is still no teaching or suggestion for executing a software routine to determine a maximum number of memory devices that can be supported per memory bus channel and "automatically" determine memory upgrade options..." Examiner notes that the claim language does not require a software routine to do so – indeed, it would not be patentable if it did, under 35 USC 101 – software is not patentable, per se. In addition, merely automating a known task is also not patentable.

As applicants discuss at page 5 of the instant specification, RAMBUS controllers are known to support a certain maximum number of devices. Any "determination," absent some new method for determining disclosed by applicant (which it is not), may simply be anticipated by the installer counting the number of controllers and multiplying the slots by the number of controllers, for example.

In conclusion, the determination is either not enabled and described as some new method of determining, or is not patentable over the applied prior art.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christian P. Chace whose telephone number is 571.272.4190. The examiner can normally be reached on MAXI FLEX.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Reginald Bragdon can be reached on 571.272.4204. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Christian P. Chace
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Art Unit 2189